

SHIOTA ET AL. - 10/706,266
Client/Matter: 061063-0306825

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A silicon wafer wherein stacking fault nuclei are distributed throughout the entire in-plane direction, and a density of said stacking fault nuclei is set to a range of between $0.5 \times 10^8 \text{ cm}^{-3}$ and $1 \times 10^{11} \text{ cm}^{-3}$.

2. (Previously presented) A silicon wafer according to claim 1, which is cut from an ingot formed from a perfect region wherein interstitial silicon-type point defect agglomerates and vacancy-type point defect agglomerates are substantially non-existent.

3. (Original) A silicon wafer according to claim 1, which is cut from an ingot formed from a region wherein vacancy-type point defects are dominant.

4. (Previously presented) A manufacturing method of a silicon wafer, comprising pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing the ingot to manufacture the silicon wafer according to claim 1,

wherein said ingot is pulled such that a ratio V/G of, a rate V at which the ingot is pulled, and a temperature gradient G of the ingot in the vertical direction in the vicinity of an interface between the silicon melt in the crucible and the ingot, is between $0.20 \text{ mm}^2/\text{^{\circ}C}\cdot\text{minute}$ and $0.25 \text{ mm}^2/\text{^{\circ}C}\cdot\text{minute}$.

5. (Previously presented) A manufacturing method of a silicon wafer, comprising pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing the ingot to manufacture the silicon wafer according to claim 1,

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wherein nitrogen is added while pulling said ingot, to set an internal nitrogen concentration within a range of between $5 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{15} \text{ cm}^{-3}$.

6. (Previously presented) A manufacturing method of a silicon wafer which manufactures the silicon wafer according to claim 1, comprising:

vacancy heat treating for forming new vacancies in the interior by means of a heat treatment of said silicon wafer in an atmosphere gas containing nitrogen; and

SF nuclei heat treating which agglomerates interstitial silicon released during precipitation of oxygen from vacancies injected by said vacancy heat treatment step, to form stacking fault nuclei,

and a temperature in said SF nuclei heat treating is above 1100°C, and is increased at a rate of not more than 10°C/minute.

7. (Previously presented) A manufacturing method of a silicon wafer according to claim 6, wherein an oxide film on the surface of said silicon wafer is removed prior to said vacancy heat treating.

8. (Previously presented) A manufacturing method of a silicon wafer according to claim 6, wherein during said vacancy heat treating, purging is conducted to remove oxygen from the atmosphere gas surrounding said silicon wafer, and said silicon wafer is quenched after said vacancy heat treating.

9. (Previously presented) A manufacturing method of a silicon wafer comprising heat treating to the silicon wafer according to claim 1, to form at least a defect-free layer on the surface of said silicon wafer.

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10. (Previously presented) A silicon wafer manufactured by the method of claim 9.

11. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer according to claim 2, to form at least a defect-free layer on the surface of said silicon wafer.

12. (Original) A silicon wafer manufactured by the method of claim 11.

13. (Currently amended) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer ~~manufactured by the method of~~ according to claim 3, to form at least a defect-free layer on the surface of said silicon wafer.

14. (Original) A silicon wafer manufactured by the method of claim 13.

15. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 4, to form at least a defect-free layer on the surface of said silicon wafer.

16. (Original) A silicon wafer manufactured by the method of claim 15.

17. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 5, to form at least a defect-free layer on the surface of said silicon wafer.

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18. (Original) A silicon wafer manufactured by the method of claim 17.

19. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 6, to form at least a defect-free layer on the surface of said silicon wafer.

20. (Original) A silicon wafer manufactured by the method of claim 19.

21. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 7, to form at least a defect-free layer on the surface of said silicon wafer.

22. (Original) A silicon wafer manufactured by the method of claim 21.

23. (Original) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 8, to form at least a defect-free layer on the surface of said silicon wafer.

24. (Original) A silicon wafer manufactured by the method of claim 23.